



US 20020164118A1

(19) **United States**(12) **Patent Application Publication**
Paddon et al.(10) **Pub. No.: US 2002/0164118 A1**(43) **Pub. Date: Nov. 7, 2002**(54) **PHOTONIC INPUT/OUTPUT PORT**

on Jun. 29, 2001. Provisional application No. 60/332,339, filed on Nov. 21, 2001.

(76) **Inventors:** **Paul J. Paddon**, Vancouver (CA);
Michael K. Jackson, Richmond (CA);
Jeff F. Young, North Vancouver (CA);
Selena Lam, Vancouver (CA)**Publication Classification**(51) **Int. Cl.⁷** **G02B 6/26; G02B 6/10**(52) **U.S. Cl.** **385/31; 385/39; 385/141; 385/129**

Correspondence Address:

Dean A. Pelletier**McAndrews, Held & Malloy, Ltd.****34th Floor****500 West Madison Street****Chicago, IL 60661 (US)**(57) **ABSTRACT**

The present I/O ports comprise (1) a layered structure comprising (a) an unpatterned superstrate having at least one layer, (b) an unpatterned substrate having at least one layer, and (c) at least one intermediate layer sandwiched between the unpatterned superstrate and the unpatterned substrate, (2) a coupling region that is within the at least one intermediate layer and that comprises an arrangement of at least one optical scattering element and (3) at least one output waveguide. The present I/O ports can be effectively used in balanced photonic circuits and unbalanced photonic circuits.

(21) **Appl. No.:** **10/109,302**(22) **Filed:** **Mar. 28, 2002****Related U.S. Application Data**

(60) Provisional application No. 60/281,650, filed on Apr. 5, 2001. Provisional application No. 60/302,256, filed

